Rajit Manohar

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Education:

Ph.D. 1998	Computer Science, California Institute of Technology
M.S. 1995	Computer Science, California Institute of Technology
B.S. 1994	Engineering and Applied Science, California Institute of Technology
1990–92	Computer Science and Engineering, Indian Institute of Technology, Bombay

Professional Experience:

1/2017–	John C. Malone Professor of Electrical & Computer Engineering Secondary appointment: Computer Science Secondary appointment: Applied and Computational Mathematics *Started the Computer Systems Lab*	Yale University
8/1998– 12/2016	Assistant, Associate, and Full Professor, ECE *Started the Computer Systems Lab*	Cornell University
1/2015	Stephen H. Weiss Presidential Fellow	
7/2012	Professor, Cornell Tech	

Administrative

7/2024–	Deputy Dean for Innovation and Entrepreneurship *School of Engineering and Applied Science*	Yale University
1/2023– 6/2014	Deputy Dean for Research *School of Engineering and Applied Science (inaugural appointment)*	Yale University
1/2015– 4/2015	Associate Dean for Research *Cornell Tech, New York City*	Cornell University
11/2012– 12/2014	Associate Dean for Academic Affairs *Cornell Tech, New York City (inaugural appointment)*	Cornell University
1/2010– 6/2012	Associate Dean for Research & Graduate Studies *College of Engineering*	Cornell University

Other

8/2005– 12/2005	Visiting Scientist *Microsystems Technology Laboratories*	Massachusetts Institute of Technology
2004–2010	Founder and CTO *On leave from Cornell, 8/2005–7/2007*	Achronix Semiconductor

Honors and Awards:

Paper recognition:

2025 Best student paper nominee, International Symposium on Nonlinear Theory and Its Applications
For "DOIM50: A 50-Spin Fully Connected Oscillator Ising Machine IC for MU-MIMO Detection."

2024 Paper selected for IEEE Micro Top Picks from Computer Architecture Conferences
For "SCALO: An Accelerator-Rich Distributed System for Scalable Brain-Computer Interfacing."

2023 Best paper award, ASYNC (*one paper selected each year*)
For "Timed Signaling Processes."

2023 Best paper nominee, ASYNC (*three papers nominated each year*)
For "Opportunistic Mutual Exclusion."

2023 Paper selected for ISCA-50's 25-year retrospective
For "Hardware-Software Co-Design for Brain Computer Interfaces." Papers selected from the past 25 years of the ISCA conference.

2023 Best paper award, ISCA (*two papers selected*)
For "SCALO: An Accelerator-Rich Distributed System for Scalable Brain-Computer Interfacing."

2021 Best paper nominee, ASYNC
For "Fluid: An Asynchronous High-level Synthesis Tool for Complex Program Structures."

2021 Paper selected for IEEE Micro Top Picks from Computer Architecture Conferences
For "Hardware-Software Co-Design for Brain-Computer Interfaces."

2020 Best paper award, ASYNC
For "Cyclone: a static timing and power analysis engine for asynchronous circuits."

2019 Best paper nominee, ASYNC
For "AMC: An Asynchronous Memory Compiler."

2017 Best paper nominee, ASYNC
For "The Eventual C-Element Theorem for Delay-Insensitive Asynchronous Circuits."

2016 Best paper nominee, ASYNC
For "Gradual Synchronization."

2016 IBM Research 2014 Pat Goldberg Math/CS/EE Best Paper Award (first place)
For "A Million Spiking-Neuron Integrated Circuit with a Scalable Communication Network and Interface." Selected annually from papers with IBM co-authors.

2016 "Best of Computer Architecture Letters" in 2015 (*four papers selected*)
For "Comparing Stochastic and Deterministic Computing."

2015 Best paper nominee, ASYNC
For "Analyzing Isochronic Forks with Potential Causality."

2014 Best paper nominee, ASYNC
For "Low Power Asynchronous VLSI with NEM Relays."

2013 Best paper award, ASYNC
For "Inverting Martin Synthesis for Verification."

2012 Best paper award, ASYNC
For "A Digital Neurosynaptic Core Using Event-Driven QDI Circuits."

2010 Best paper award, ASYNC
For "An Operand-Optimized Asynchronous IEEE 754 Double-precision floating-point adder."

2010 Best paper nominee, ASYNC
For "An Asynchronous FPGA with Two-Phase Enable Scaled Routing."

2007 Best paper award, High Performance Embedded Computing
For "Enabling Cognitive Architectures for UAV Mission Planning."

2006 Best paper award, ASYNC

For "A level-crossing Flash Asynchronous Analog-to-Digital Converter."

2005 Best paper nominee, ASYNC
For "BitSNAP: Dynamic Significance Compression for a Low-Energy Sensor Network Asynchronous Processor."

2005 IEEE Fred Ellersick Award for best unclassified paper at MILCOM
For "Dense Sensor Networks are also Energy-efficient: when more is less."

2004 Best paper award, IASTED Parallel and Distributed Computing and Systems
For "Δ-dataflow networks for event-stream processing."

Research and Technology:

2022 IEEE Fellow
For "contributions to the design and implementation of asynchronous circuits and systems."

2016 TrueNorth neuromorphic chip inducted into the Computer History Museum

2016 Inaugural Misha Mahowald Prize for Neuromorphic Engineering
For the TrueNorth project with IBM Research. The prize is for "outstanding research in neuromorphic engineering, worldwide" and is awarded to a project.

2015 R&D 100 Award for the TrueNorth project in the IT/Electrical category

2015 Invited "keynote" paper, IEEE Transactions on CAD
Paper: "TrueNorth: Design and Tool Flow of a 65mW 1 Million Neuron Programmable Neurosynaptic Chip."

2014 ACM Gordon Bell Prize finalist, Supercomputing
For "Real-time Scalable Cortical Computing at 46 Giga-Synaptic OPS/Watt with $\approx$100$\times$ Speedup in Time-to-Solution and $\approx$100,000$\times$ Reduction in Energy-to-Solution."

2009 IET Start-up Innovation Award, Achronix Semiconductor
For development of asynchronous FPGA technology.

2006 Elected Fellow of the World Technology Network

2006 Globus Indus Technovators Award

2006 Invited participant, NAE Frontiers of Engineering Symposium

2005 MIT Technology Review's TR35: top 35 young innovators under 35
For contributions to low power microprocessor design.

2001 MIPS paper in Caltech Computer Science 25$^{\text{th}}$ Anniversary Selected Bibliography
Each Caltech CS faculty member selected two papers from their career.

2000 NSF CAREER award

1996 National Semiconductor Corporation Graduate Fellowship

1993 Caltech Merit Award

1992 IIT Bombay Academic Award for being ranked 1$^{\text{st}}$ in the Institute

1991 IIT Bombay Academic Award for being ranked 1$^{\text{st}}$ in the Institute

1990 Gold Medal, National Standard Examination in Physics, India

Teaching:

2016 Professor of the Year at Cornell Tech
Selected by the Cornell Tech student body; three per year across all degree programs.

2014 Stephen H. Weiss Presidential Fellow
For "a sustained record of effective, inspiring, and distinguished teaching of undergraduate students." Cornell's highest teaching honor and a permanent designation.

2012 Kenneth A. Goldman '71 Excellence in Teaching Award
One of multiple named teaching awards in the College of Engineering at Cornell.

2009 Ruth and Joel Spira Excellence in Teaching Award

Cornell ECE departmental teaching award.

2005 Ruth and Joel Spira Excellence in Teaching Award
Cornell ECE departmental teaching award.

2004 Michael Tien '72 Excellence in Teaching Award
One of multiple named teaching awards in the College of Engineering at Cornell.

2001 Sonny Yau '72 Excellence in Teaching Award
One of multiple named teaching awards in the College of Engineering at Cornell.

2001 Cornell University IEEE Teacher of the Year Award
Selected by the undergraduate IEEE student chapter.

2000 Tau Beta Pi and Cornell Society of Engineers Excellence in Teaching Award
One per year in the College of Engineering, selected by direct student vote.

Member: Tau Beta Pi; Sigma Xi; IEEE; ACM

Professional Activities:

Academic:

Steering Committee Member
Bangalore Neuromorphic Engineering Workshop, 2025–
IEEE International Symposium on Asynchronous Circuits and Systems, 2007–2012, 2020–

Associate Editor
IEEE Transactions on VLSI, 2007–2009

Program Co-Chair
11th IEEE International Symposium on Asynchronous Circuits and Systems, March 2005

Program Topic Co-Chair
Conference on Design, Automation and Test in Europe, March 2003

Co-Organizer
Kavli Institute Symposium on Computing Challenges, Cornell, October 2008
Address-Event Workgroup, NSF Workshop on Neuromorphic Engineering, Telluride, CO, July 2000

Program Committees
ACM Multimedia Workshop on asynchronous video (2023); Asia and South Pacific Design Automation Conference (2016–2018); IEEE International Conference on Event-based Control, Communication, and Signal Processing (2015–2017); IEEE International Symposium on Asynchronous Circuits and Systems, (2001–present); International Conference on Nano-Networks (2008-09); International Conference on Computer Design (2006); International Conference on Computer Aided Design (2005); Conference on Design, Automation and Test in Europe (2005, 2024-26); International Conference on Supercomputing (2002); Workshop on Open-Source EDA Technology (2020–22, 2024)

Reviewer: Proposals and Funded Projects
Air Force Research Labs; Agency for Science, Technology, and Research, Singapore; Army Research Office; US-Israel Bi-national Science Foundation; Defense Threat Reduction Agency; Israel Science Foundation; IWT Brussels, Belgium; National Science Foundation (US); National Institutes for Health (US); Natural Sciences and Engineering Research Council, Canada; Netherlands Organization for Scientific Research; Research Grants Council of Hong Kong; Singapore National Research Foundation; Swiss National Science Foundation; Quantum Science Austria

Journal Reviewer
ACM Transactions on Design Automation of Electronic Systems (TODAES); ACM Transactions on Programming Languages and Systems (TOPLAS); ACM Transactions on Reconfigurable Technology and Systems (TRETS); ACM Computing Surveys; Communications of the ACM (CACM); Formal Aspects of Computing (FAC); IEEE Computer; IEEE Journal of Solid-State Circuits (JSSC); IEEE Signal Processing Letters; IEEE Transactions on Biomedical Circuits and Systems (TBioCAS); IEEE Transactions on Circuits and Systems (TCAS I and II); IEEE Transactions on Computer Aided Design (TCAD); IEEE Transactions on Computers (TC); IEEE Transactions on Parallel and Distributed Systems (TPDS); IEEE Transactions on VLSI (TVLSI); IET Computers and Digital Techniques; Information Processing Letters (IPL); INTEGRATION: The VLSI Journal; Nature Communications; Neural Computation (NECO); Philosophical Transactions A; Proceedings of the IEEE (PIEEE); Science; Science Advances

Conference Reviewer
Conference on Advanced Research in VLSI (ARVLSI); International Symposium on Asynchronous Circuits and Systems (ASYNC); Design Automation Conference (DAC); European Conference on Parallel and Distributed Computing (EuroPar); International Symposium on High Performance Computer Architecture (HPCA); International Parallel Processing Symposium (IPPS); International Parallel and Distributed Processing Symposium (IPDPS); International Symposium on Computer Architecture (ISCA); International Symposium on Microarchitecture (MICRO); International Conference on Parallel Architectures and Compilation Techniques (PACT); ACM Symposium on Principles of Distributed Computing (PODC); ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI); ACM Special Interest Group on Data Communication (SIGCOMM); International Symposium on Operating System Principles (SOSP)

External Search Committee Member
Member of search committee for hiring chaired professors at multiple European universities.

External Review Committee Member
Department of Electrical and Computer Engineering, Boston University

External Advisory Board Member
National Science Foundation National Chip Design Hub, 2025–

Technology Transfer/Consulting:

Founder, Opus Semiconductor LLC
Startup company commercializing asynchronous logic and tools.

Microservices acceleration, Intel
Consulting on hardware and software for microservices leveraging Intel's CPU and IPU. 8/2021–12/2022

Founder and CTO, Achronix Semiconductor
Startup company commercializing high-speed asynchronous FPGAs.
CTO 10/2004–12/2008; Chief Scientist 12/2008–4/2010; Board of Directors 10/2004–3/2011.

Asynchronous Design Tools and Methodology
Design methodologies and automation tools developed by my group used by external groups at (i) over a dozen companies including Achronix Semiconductor, IBM Research, Qualcomm, Google, Femtosense, Galois, Infineon, Opus Semiconductor, and Intel; (ii) over a dozen research organizations including Stanford University, Tsinghua University, ETH Zurich, Johns Hopkins University, TU Wien, University of Groningen, Lawrence Livermore National Labs, and Brookhaven National Labs.

Other Activities
ATC-NY. Asynchronous logic synthesis (DARPA/SBIR). 1/2003–9/2003

Insect-Cyborg Sentinels: Technology Transfer Activity (DARPA). 6/2009–3/2011

Samraksh, Inc. FPGAs for embedded system security (AFRL/STTR) 2017–2019

Technical Advisory Board, Kepler, 2018–

Scientific Advisor, Volantis, 2021–

Scientific Advisor, Ludwig, 2023–

Scientific Advisor, xMentium, 2024–

Invited Talks/Sessions:

Research

A Full-Stack Neuromorphic System Implementation for Development and Benchmarking.
Keynote, 2026 DOE Energy Consequences of Information Workshop, February 2026.

Asynchronous FPGAs: From Technology to a Business.
Center for Development of Advanced Computing, Bengaluru, India, January 2026.

Neuromorphic computing: a systems perspective.
Keynote, Bangalore Neuromorphic Engineering Workshop, January 2026.

Communication cost in neuromorphic systems.
SFI working group on Neuromorphic Stochastic Thermodynamics, Santa Fe, NM, December 2025.

The role of time in digital logic.
Applied Mathematics Seminar Series, Yale University, December 2025.

Future of System Architectures.
Panelist, DOE Workshop on Modeling & Simulation of Systems and Applications, August 2025.

Self-timed Logic: Design and Automation.
Telluride Neuromorphic Cognition Engineering Workshop, July 2025.

A Flexible Testbed for Neuromorphic Computing.
Engineering session, "Neuromorphic Testbeds: Pioneering Energy-Efficient Computing for the Future," Design Automation Conference, June 2025.

Self-timed systems for energy-efficient computing.
Royal Society scientific meeting on "Bits, Neurons, and Qubits for Sustainable AI.", April 2025.

Introduction to Asynchronous Computing.
Seminar, Indian Institute of Technology, Mumbai, India, January 2025.

Self-timed Neuromorphic Systems.
Bangalore Neuromorphic Engineering Workshop, Indian Institute of Sciences, January 2025.

Self-timed Neuromorphic Systems.
Seminar, Department of Computer Science, University of Notre Dame, IN, December 2024.

The ACT EDA flow for asynchronous logic.
Seminar, IBM T.J. Watson Research Center, Yorktown Heights, NY, July 2024.

The ACT EDA flow for asynchronous logic.
Free Silicon Conference, Paris, France, June 2024.

A unified theory of time and causality for digital logic.
Seminar, University of California at Berkeley, Berkeley CA, May 2024.

Neuromorphic Computing with Symbols.
1st International Conference on Neuro-symbolic Systems, Berkeley, CA, May 2024.

Full-stack Design of Neuromorphic Systems.
Seminar, University of Connnecticut, Storrs, CT, February 2024.

Inference in Chip Design.
Yale Inference Workshop, hosted by the Franke Program in Science and the Humanities and the John Templeton Foundation, December 2023.

Asynchronous Logic: Design and EDA.
Seminar, IEEE Circuits and Systems Rio Grande do Sul Chapter, September 2023.

Evaluating Neuromorphic Algorithms on Neuromorphic Substrates.
COINFLIPS seminar, Sandia National Labs, August 2023.

Toward Programmable CMOS Ising Machines.
Telluride Neuromorphic Cognition Engineering Workshop, July 2023.

Full stack Co-design for Neuromorphic Systems.
Neuro-Inspired Computing Elements Conference, April 2023.

Asynchronous Circuits for Large-scale Neuromorphic Systems.
Telluride Neuromorphic Cognition Engineering Workshop, July 2022.

Event-driven hardware for brain-computer interfaces.
Yale Clinical Neuroscience Grand Rounds, May 2022.

Hardware/software co-design for Neuromorphic Systems.
IEEE Custom Integrated Circuits Conference, April 2022.

An ASIC flow for asynchronous logic.
Seminar for the ASIC & VLSI Research group, NVIDIA Research, November 2021.

An Open-source ASIC flow for asynchronous logic.
DARPA ERI Summit Panel, October 2021.

Using chiplets to enable a firmware app store.
Workshop organized by the Open Domain-Specific Architecture workgroup of the Open Compute Project, August 2021.

The impact of new devices on neuromorphic systems and in-memory computing.
Panelist, NSF Workshop on Devices to Systems for In-Memory Computing, May 2021.

Asynchronous Logic: Design and Automation.
CIRCT weekly disussion group, February 2021.

Challenges in AI/ML/neuromorphic hardware design.
Panelist, NSF Workshop on Electronic Design & Automation: Challenges & Opportunities, Dec 2020.

Asynchronous Logic: Design and EDA.
Hardware Seminar, University of California at Santa Cruz, Santa Cruz, CA, December 2020.

Self-Timed Neuromorphic Systems.
Design Automation Conference Workshop on Neuromorphic Computing, June 2020.

Neuromorphic Systems: from concept to design.
ACRC Research Day, Technion, January 2020.

Integrated verification and synthesis of asynchronous circuits.
New England Systems Verification Day, MIT, October 2019.

Architectures for Neuromorphic Computing.
DOE Workshop on Modeling & Simulation of Systems and Applications, August 2019.

Neuromorphic Computing.
New York Scientific Data Summit, Columbia University & Brookhaven National Labs, June 2019.

Open-source design tools for asynchronous circuits.
Panelist, NII Shonan Meeting on Asynchronous Design, Japan, May 2019.

Teaching asynchronous design: from principles to tapeout in a semester.
NII Shonan Meeting on Asynchronous Design, Japan, May 2019.

Computing with Events.
Yale Day of Instrumentation, November 2018.

Design Automation for Asynchronous Circuits.
IEEE CASS Seasonal School on Logic Synthesis, Porto Alegre, Brazil, August 2018.

Computing without clocks.
Yale Science and Engineering Forum, May 2018.

Scalable Routing in Large Scale Neuromorphic Systems.
*A*STAR Neuromorphic Computing Workshop, Singapore, March 2018.*

Hybrid CMOS/NEMS for Neuromorphic Engineering.

IEEE MEMS Bay Area Section meeting, Santa Clara, CA, August 2017.

Self-Timed Systems and their Application to Neuromorphic Computing.
Google, Sunnyvale, CA, August 2017.

NEMS for Neuromorphic Computing.
Napa Microsystems Workshop, Napa, CA, August 2017.

Neuromorphic Computing—Do Devices Matter?
Device Research Conference rump session panel member, Notre Dame, IN, June 2017.

Bio-inspired learning and inference systems: what went well and what didn't.
Panelist, IEEE Custom Integrated Circuits Conference, Austin, TX, May 2017.

Neuromorphic Computer Systems.
Keynote, 26th Connecticut Microelectronics & Optoelectronics Symposium, Storrs, CT, April 2017.

Stochastic vs Deterministic Computing.
Panelist, International Conference on Computer-Aided Design, Austin, TX, November 2016.

Neuromorphic Systems: Past, Present, and Trends.
Physics Seminar Series, IBM T.J. Watson Research Center, Yorktown Heights, NY, September 2016.

Large-Scale Neuromorphic Systems.
*Invited talk, A*STAR Neuromorphic Computing Workshop, Singapore, August 2016.*

Design Automation Challenges in Neuromorphic Systems.
Keynote, 25th International Workshop on Logic and Synthesis, Austin, TX, June 2016.

Neuromorphic Systems.
Seminar, Reservoir Labs, New York, NY, May 2016.

Comparing Stochastic and Deterministic Computing.
Best of Computer Architecture Letters Session,
IEEE Symposium on High-Performance Computer Architecture, Barcelona, Spain, March 2016.

Asynchronous Logic: A Computer Systems Perspective.
Neuro-Inspired Computational Elements (NICE) Workshop, Berkeley, CA, March 2016.

Large-Scale Neuromorphic Systems.
Triangle Computer Science Distinguished Lecturer Series, UNC/NCSU/Duke, November 2015.

Designing Massively Parallel Computing Architectures.
Neuromorphic Computing Forum, SAIT, Samsung, Korea, November 2015.

Engineering Neuromorphic Systems.
Center for Neuroengineering and Computation, Columbia University, New York, NY, September 2015.

Self-timed Neuromorphic Systems.
Computer Engineering Seminar Series, Yale University, New Haven, CT, September 2015.

Neuromorphic Systems: Past, Present, and Trends.
Computer Science Seminar, Columbia University, New York, NY, July 2015.

Digital Neuromorphic Systems.
Seminar, University of California at Berkeley, Berkeley, CA, May 2015.

Digital Neuromorphic Systems.
Workshop on Neuromorphic and Brain-based Computing Systems, Design, Automation & Test in Europe, Grenoble, France, March 2015.

Digital Neuromorphic Systems.
Physiology, Biophysics and Systems Biology Seminar, Weill Medical College, New York, NY, January 2015.

Energy Proportional Computing.
Cornell Systems-Industry Workshop, Ithaca, NY, November 2014.

Self-timed Neuromorphic Systems.

Brain-Inspired Computing, Cognitive Systems Colloquium, IBM Almaden Research Center, November 2014.

Digital Neuromorphic Electronics.
Seminar, Brain and Mind Institute, Weill Medical College, New York, NY, June 2014.

Energy-efficient self-timed circuits.
Seminar, Advanced Micro Devices, Boxborough, MA, October 2013.

Self-timed Logic for Neuromorphic Systems.
Joint EU-US Workshop on Cortical Processors, Heidelberg, Germany, October 2013.

Low power embedded systems using self-timed circuits.
Seminar, Intel STC on Embedded Computing, April 2013.

Self-timed systems: Case Studies.
2012 Kyoto Prize Symposium on Asynchronous computing, San Diego CA, March 2013. (Symposium held in honor of Ivan Sutherland)

Energy-efficient Self-timed Systems.
Qualcomm Research Center, NJ, March 2013.

Asynchronous VLSI Design.
Olin College, MA, November 2012.

Energy-Efficient Self-Timed Systems.
Case Western Reserve University, Cleveland, OH, October 2012.

Scalable Routing in Large-Scale Neuromorphic Systems.
IEEE International Conference on Engineering in Medicine and Biology
Mini-symposium on Large-scale Neuromophic Systems, August 2012.

High Performance Reconfigurable Logic.
Indian Institute of Technology, Mumbai, India, January 2012.

Digital Neuromorphic Systems.
IBM T.J. Watson Research Center, Yorktown Heights, NY, November 2011.

Asynchronous Computer Arithmetic.
Architecture seminar series, University of Wisconsin, Madison, WI, November 2011.

Ultra Low Power Computation for Secure Embedded Systems.
TRUST Autumn Conference, Washington, DC, November 2011.

Efficient floating-point: software and hardware.
Scientific Computing and Numerics Seminar, Cornell University, October 2011.

Low Power Asynchronous VLSI.
Huawei Research, Ontario, Canada, May 2011.

Activity-Driven Architecture for Neuromorphic Systems.
DARPA Neural Engineering, Science, and Technology Forum, San Diego, CA, November 2010.

Asynchronous VLSI Design.
Olin College, MA, November 2010.

Asynchronous FPGAs: An Overview.
KLA-Tencor, Milpitas, CA, October 2010.

The Technology and Business of Asynchronous FPGAs.
University of California at Berkeley, Berkeley CA, October 2010.

Self-Timed FPGAs.
Portland State University, Portland, OR, September 2010.

Reconfigurable Systems.
CS Colloquium, Cornell University, September 2010.

GHz-speed FPGAs.
CMOS Emerging Technologies Workshop, Whistler, BC, May 2010.

High-performance Reconfigurable Systems.
Visionary and Entrepreneurship Seminar, ECE, UC Davis, CA. February 2010.

The Future of FPGAs.
High Performance Embedded Computing, MIT Lincoln Labs, September 2009.

Survivor: Computer Architecture.
Panelist, High Performance Embedded Computing, MIT Lincoln Labs, September 2009.

VLSI Systems: Past, Present, and Future Trends.
California Institute of Technology, Pasadena, CA, February 2009.

Managing Design Complexity in VLSI Systems.
University of Texas at Austin, TX, February 2009.

Fault Tolerance in Asynchronous Logic.
University of Texas at Austin, TX, February 2009.

Fault Tolerance in Asynchronous Logic.
Integrated Systems Lab Seminar, Columbia University, NY, December 2008.

An Ultra Low Power Processor for Sensor Networks.
Computer Engineering Seminar, University of Texas at Austin, TX, November 2008.

Event-Driven Computing.
Center for Highly Integrated Physical Systems, Ithaca, NY, October 2008.

Fault Tolerance in Reconfigurable Fabrics.
Schloss Dagstuhl-Leibniz Center for Informatics, Wadern, Germany, September 2008.

The 50 billion transisistor challenge.
IBM Global Technology Outlook Workshop, Yorktown Heights, NY, July 2008.

Ultra Low Power Asynchronous Systems.
IBM Almaden Research Labs, San Jose, CA, June 2008.

Microprocessor Forum.
Panelist, Gilder-Forbes Telecosm Conference, Lake George, NY, May 2008.

The Critical Path of Fiberspeed Connectivity: Flexible vs Fixed Silicon Solutions.
Panelist, Gilder-Forbes Telecosm Conference, Lake George, NY, October 2007.

The Implications of Fast Asynchronous Reconfigurable Logic.
DSRC Workshop on Terascale Integration, Washington, DC, October 2007.

3D Integrated Circuits: A Designer's Perspective.
Keynote panelist, 24th VLSI Multilevel Interconnection Conference. Fremont, CA, September 2007.

Fast Reconfigurable Logic.
Yale University, September 2007.

Asynchronous FPGAs.
Keynote, Workshop on Unique Chips and Systems, San Jose, CA, April 2007.

Reconfigurable Asynchronous Logic.
University of Texas at Austin, Austin, TX, March 2007.

Asynchronous Embedded Systems.
Welch-Allyn, Skeneateles, NY, March 2007.

Asynchronous Circuits and Systems.
Pomona College, CA, November 2006.

Reconfigurable Asynchronous Logic.
Custom Integrated Circuits Conference, San Jose, CA, September 2006.

Self-timed Systems.
Microsystems Technology Labs, MIT, Boston, MA, December 2005.

Reconfigurable Asynchronous Logic.
Columbia University, New York, NY, December 2005.

Asynchronous FPGAs.
Air Force Rome Labs, Rome, NY, October 2005.

Reconfigurable Asynchronous Logic.
Olin College, MA, October 2005.

Architectures for Cognitive Systems.
Workshop on Cognitive Architectures and Systems, Ithaca, NY, July 2005.

Hardware/software co-design for Sensor Networks.
Second International Workshop on Networked Sensing Systems, San Diego, CA, June 2005.

Asynchronous Logic for Extreme Environments.
University of Central Florida, Orlando, FL, May 2005.

Asynchronous FPGAs.
Xilinx Research Labs, San Jose, CA, April 2005.

Asynchronous FPGAs.
IBM T.J. Watson Research Center, Yorktown Heights, NY, March 2005.

Activity-Driven Asynchronous Circuits and Systems.
IGERT Seminar on Machines and Organisms, Ithaca, NY, February 2005.

Issues in the Design of Sensor Network Processors.
NSF Meeting on Networks of Sensor Systems, October 2004.

Sensor Networks and Asynchronous VLSI.
IEEE Computer Society Symposium on VLSI, February 2004.

How Asynchronous should we be.
Invited panelist, IEEE Computer Society Symposium on VLSI, February 2004.

Ultra Low Power Asynchronous VLSI.
DARPA Workshop on Ultra Low Power Technologies, MIT, January 2004.

Asynchronous Event-Processing.
Analog and Biological VLSI Systems Seminar, MIT, November 2003.

SNAP: A Sensor Network Asynchronous Processor.
Electrical and Systems Engineering Colloquium, University of Pennsylvania, October 2003.

Designing an Efficient Sensor Network Processor.
VLSI seminar series, ECE, Cornell University, September 2003.

Modeling Wireless Networks with Asynchronous VLSI.
Information Sciences Seminar, California Institute of Technology, Pasadena, CA, June 2002.

Why we should design asynchronous circuits.
Intel Microprocessor Research Labs, Hillsboro, OR, April 2002.

Network Simulation with Asynchronous VLSI.
Portland State University, Portland, April 2002.

Network Simulation with Asynchronous VLSI.
AT&T Labs, Menlo Park, January 2002.

Scalable Formal Design Methods for Asynchronous VLSI.
Keynote, ACM SIGPLAN Symposium on Principles of Programming Languages, January 2002.

Asynchronous VLSI for Wireless Communication Systems.
Plenary talk, IEEE CAS Workshop on Wireless Communications and Networking, August 2001.

Low Energy Adaptive Processors.
Cornell Computer Science Distinguished Lecture Series, Ithaca, NY, September 2000.

Asynchronous VLSI Design.
NSF Workshop on Neuromorphic Engineering, Telluride, CO, July 2000.

A Methodology for Designing Asynchronous Circuits.
PRL Seminar, Cornell, January 1999.

Slack Elasticity in Asynchronous Systems.
Compaq's Systems Research Center, Palo Alto, CA, April 1998.

High-performance asynchronous microprocessors.
Cornell University (and others), March 1998.

The design of asynchronous adders.
Seminar, ECE Department, Johns Hopkins University, June 1997.

Quasi-Delay-Insensitive Circuits are Turing-Complete.
International Symposium on Asynchronous Circuits and Systems, March 1996.

Asynchronous Circuit Design.
DEC Systems Research Center, Palo Alto, September 1995.

General, IP and Tech Transfer

Introduction to Asynchronous Computing.
Beaver Works Summer Institute, Lincoln Labs, MIT, July 2025.

Introduction to Asynchronous Computing.
Beaver Works Summer Institute, Lincoln Labs, MIT, August 2024.

The computing revolution enabling AI Systems.
Yale Alumni Weekend, May/June 2024.

IP Strategies for Technology Entrepreneurs.
Panel, Future of Urban Innovation Summit, Columbia University, New York, NY, June 2015.

Cornell Tech Overview.
Cornell Systems-Industry Workshop, Ithaca, NY, November 2014.

Cornell NYC Tech.
ECE Department Heads Association Board of Directors Meeting, New York, NY, July 2013.

Cornell NYC Tech: New Directions in Building Human Capital.
The New York Academy of Sciences, New York, NY, April 2013.

The Cornell NYC Tech Campus.
IBM T.J. Watson Research Center, NY, March 2013.

Generation Tech: Tapping NYC's Science and Engineering Talent.
Panel discussion, The New York Academy of Sciences, New York, NY, November 2012.

Tutorials:

Third Summer School on Asynchronous Design.
IEEE International Symposium on Asynchronous Circuits and Systems, June 2026.
With: *in planning*

Self-timed logic: Design and Automation.
Bangalore Neuromorphic Engineering Workshop, Bengaluru, India, January 2026.

The ACT flow for designing asynchronous systems.
Neuromorphic Cognition Engineering Workshop, Telluride, CO, July 2025.

The ACT flow for designing asynchronous logic.
Bangalore Neuromorphic Engineering Workshop, Bengaluru, India, January 2025.

Second Summer School on Asynchronous Design.
IEEE International Symposium on Asynchronous Circuits and Systems, June 2024.
With: Benjamin Hill, Montek Singh, Alex Yakovlev, Ole Richter, Filip Hormot

Open-source neuromorphic circuit design: Overview, trends, and opportunities.
IEEE European Solid-State Circuits Conference, September 2023.
With: Charlotte Frenkel, Jason Eshraghian

An ASIC flow for Asynchronous Logic.
IEEE International Symposium on Asynchronous Circuits and Systems, July 2023.

The ACT flow for designing asynchronous systems.
Neuromorphic Cognition Engineering Workshop, Telluride, CO, July 2023.

Practical Ising Machines for Solving Hard Discrete Optimization Problems.
IEEE International Symposium on Circuits and Systems, May 2023.
With: Jaijeet Roychowdhury, Hideo Mabuchi, Masanao Yamaoka

Summer School on Asynchronous Design.
IEEE International Symposium on Asynchronous Circuits and Systems, June 2022.
With: Benjamin Hill, Marly Roncken, Montek Singh, Ivan Sutherland

Neuromorphic Asynchronous Circuits (Invited tutorial).
Neuromorphic Cognition Engineering Workshop, Telluride, CO, 2012.

Neuromorphic Asynchronous Circuits (Invited tutorial).
Neuromorphic Cognition Engineering Workshop, Telluride, CO, 2011.
With: Shih-Chi Liu

Teaching Experience:

2017– **Professor** **Yale University**

Instructor: EENG 425/ENAS 875: Introduction to VLSI System Design**
EENG 426/CPSC 459/ENAS 876: Silicon Compilation*
EENG 429: Digital VLSI Testing*
EENG 348/CPSC 338: Digital Systems**

2013–2016 **Professor** **Cornell University and Cornell Tech**

Instructor: CS 5422: Physical Computing*
CS 5460: Parallel and Distributed Computing*
CS 5191: Studio
Clinic: Mathematics for Machine Learning*

2010–2012 **Professor** **Cornell University**

Instructor: ECE 3140: Embedded Systems*
ECE 5740: Advanced Digital VLSI

2004–2010 **Associate Professor** **Cornell University**

Instructor: ECE 5740: Advanced Digital VLSI
ECE 5710: Arithmetic Circuits*
ECE 320: Systems and Networks*

1998–2004 **Assistant Professor** **Cornell University**

Instructor: ECE 574: Advanced Digital VLSI**
EE 571: Asynchronous VLSI Design*
EE 697: Topics in Computer Systems: Dynamic Binary Translation*
ECE 474: Digital VLSI Design**
EE/CS 314: Computer Organization*

Assisted: EE 439: Digital VLSI System Design
EE 308: Fundamentals of Computer Engineering
EE 475: Computer Architecture

1996–97 **Instructor** **California Institute of Technology**

Instructor: CS 139abc: Concurrency in Computation

1993–98 **Teaching Assistant** **California Institute of Technology**

Computers, Computation, and Programs (CS20, Jan L.A. van de Snepscheut); Design and Implementation of Programming Languages (CS237, Mary W. Hall); Asynchronous VLSI Design Laboratory (CS185, Alain J. Martin); Digital VLSI Design Laboratory (CS/EE181, Alain J. Martin).

Other Teaching Experience:

2015 **Curriculum Design** **Cornell Tech**
Worked with the City University of New York's Macaulay Honors College on an introductory Computer Science module for their students.

2002–2005 **Explorations in Engineering** **Cornell University**
Faculty participant in Cornell's summer program for high school juniors/seniors.

2000–2001 **CURIE Academy** **Cornell University**
Faculty participant in Cornell's summer program for high school women that excel in math and science.

1996–98 **Mentor Scientist** **Caltech Pre-College Science Initiative**
Student volunteer for Caltech's high school teacher training program.

1994–95 **CRPC Summer Intern Advisor** **California Institute of Technology**
Suggested projects/advised summer interns in the NSF Center for Research on Parallel Computation summer internship program for women and minorities.

Advising:

Current advisees:

Dr. Jakob Jordan. *4/2024–*. Topic: Computational Neuroscience and Neuromorphic Systems

Siva Nalabothu (Ph.D. ECE). *8/2025–*. Topic: Brain-computer interfaces

Kameron Gano (Ph.D. ECE). *8/2025–*. Topic: Neuromorphic computing

Karthi Srinivasan (Ph.D. ECE). *12/2022–*. Topic: Logic Synthesis for Asynchronous circuits

Thomas Jagielski (Ph.D. ECE). *8/2022–*. Topic: Ising machines

Mattia Vezzolli (Ph.D. ECE). *8/2022–*. Topic: Asynchronous linear algebra accelerators

Congyang Li (Ph.D. ECE). *1/2021–*. Topic: Neuromorphic computing

Xiayuan Wen (Ph.D. ECE). *6/2020–*. Topic: Automated synchronous to asynchronous conversion

Research staff supervised:

Ole Richter, Ph.D. University of Groningen (postdoc 2024–2025).
First employment: Assistant Professor, Danmarks Tekniske Universitet (DTU)

Rui Li, Ph.D. Yale (postdoc 2022).
First employment: Intel

Nabil Imam, Ph.D. Cornell (Research scientist 2020–2021).
First employment: Assistant Professor, Georgia Institute of Technology

Ioannis Karageorgos, Ph.D. KU Leuven (Research scientist 2019–2021).
First employment: Blue Cheetah Analog Design

Samira Ataei, Ph.D. Oklahoma State University (postdoc 2017–2019; Research Scientist 2019–2021).
First employment: Owl AI

Saber Moradi, Ph.D. ETH Zurich (postdoc 2015–2018).

$*$ New class developed; $**$ Significantly (>70%) revised existing curriculum.

First employment: Continental Silicon Valley Research Center

Carlos Tadeo Ortega Otero, Ph.D. Cornell (postdoc 2014–2015).
First employment: St. Jude Medical

Ph.D. theses supervised:

Ruslan Dashkin (Ph.D. ENAS, March 2024). *Asynchronous RISC-V CPU Design with Pre-Silicon Validation on Synchronous FPGAs.* First employment: Intel

Xiang Wu (Ph.D. CS, June 2023). *Formal Verification of an Asynchronous VLSI Flow.* First employment: Meta

Prafull Purohit (Ph.D. ECE, April 2023). *Asynchronous Circuits for Computing, Communication, and Sensing.* First employment: Brookhaven National Labs

Yihang Yang (Ph.D. ENAS, February 2022). *Custom Cell Design Placement Automation for Asynchronous VLSI.* First employment: Meta

Rui Li (Ph.D. ENAS, December 2021). *Pipelined Asynchronous High Level Synthesis for General Programs.* First employment: Intel

Zhan Liu (Ph.D. ENAS, August 2021, co-advised with Prof. T.P. Ma). *Ferroelectric* $Hf_{0.5}Zr_{0.5}O_2$*: Negative Capacitance and Wake-Up Effect.* First employment: Intel

Edward Bingham (Ph.D. ECE, December 2020). *Self-timed length-adaptive arithmetic.* First employment: Siden.io

Wenmian Hua (Ph.D. ECE, May 2020). *Cyclone: The first open-source timing and power engine for asynchronous systems.* First employment: Synopsys

Tayyar Rzayev (Ph.D. ECE, May 2019, co-advised by Prof. Albonesi). *Architectures for Intelligent Interactive Systems.* First employment: Xilinx

Benjamin Hill (Ph.D. ECE, December 2015). *Architecture and Synthesis for Dynamically Reconfigurable Asynchronous FPGAs.* First employment: Assistant Professor, Olin College

Rob Karmazin (Ph.D. ECE, November 2015). *Automating the Physical Design of Asynchronous Circuits.* First employment: Intel

Jonathan Tse (Ph.D. ECE, September 2015). *A Simple Methodology For Design Tradeoff Analysis In Asynchronous Circuits.* First employment: Intel

Stephen Longfield (Ph.D. ECE, February 2015). *Constructive Verification of Quasi Delay-Insensitive Circuits.* First employment: Google

Carlos Tadeo Ortega Otero (Ph.D. ECE, July 2014). *Asynchronous Design for Ubiquitous Computing.* First employment: St. Jude Medical

Sandra Jackson (Ph.D. ECE, July 2014). *Gradual Synchronization.* First employment: Lecturer, Colgate University

Nabil Imam (Ph.D. ECE, April 2014). *Canonical Neural Computations in Asynchronous Neuromorphic Circuits.* First employment: IBM Research

Benjamin Zhong Xian Tang (Ph.D. ECE, January 2014, co-advised by Prof. Bhave). *Exploiting Asynchrony in GPS Receiver Systems to Enable Ultra-Low-Power Operation.* First employment: Qualcomm

Basit Riaz Sheikh (Ph.D. ECE, August 2011). *Operand-Optimized Asynchronous Floating-Point Arithmetic.* First employment: CEO, CapitalTV, Pakistan (co-founder); Advisor to the Ministry of Information Technology and Telecom, Pakistan

Filipp Akopyan (Ph.D. ECE, April 2011). *Hybrid Synchronous/Asynchronous Design.* First employment: IBM Research

Christopher LaFrieda (Ph.D. ECE, December 2009). *Relaxed Quasi Delay-Insensitive Circuits.* First employment: Achronix Semiconductor Corporation

David Fang (Ph.D. ECE, May 2008). *A Profiling Infrastructure for Performance Evaluation of Asynchronous Systems.* First employment: Achronix Semiconductor Corporation

David Biermann (Ph.D. EE, September 2006). *A Workload Adaptive Voltage Scaling Multiple Clock Domain Architecture.* First employment: Intel

Song Peng (Ph.D. EE, August 2006). *Implementing Self-Healing Behavior in Quasi Delay-Insensitive Circuits.* First employment: Cadence

Virantha Ekanayake (Ph.D. EE, May 2005). *Dynamic Significance Compression in a Sensor Network Asynchronous Processor.* First employment: Assistant Professor, Johns Hopkins University

Clinton Kelly, IV (Ph.D. EE, May 2005). *The Design and Implementation of an Asynchronous Network on a Chip.* First employment: Achronix Semiconductor Corporation (co-founder)

John Teifel⋆ (Ph.D. EE, May 2004). *Fast Prototyping of Asynchronous Logic.* First employment: Senior Member of the Technical Staff, Sandia National Labs

M.S. theses supervised:

Julia Karl (M.S. ECE, December 2015). *An MSB-first Asynchronous Adder.*

Yuan Tian (M.S. ECE, May 2013). *A Parallel Implementation of Hierarchical Belief Propagation.*

Stephen Longfield (M.S. ECE, March 2013). *Design and Implementation of a Low Power Asynchronous GPS Baseband Processor.*

Carlos Otero (M.S. ECE, May 2012). *Static Power Reduction Techniques for Asynchronous Circuits.*

Nabil Imam (M.S. ECE, May 2012). *A Communication Infrastructure for Multi-Chip Neuromorphic Systems.*

Chris LaFrieda (M.S. EE, August 2005). *Custom Quality Leaf Cell Routing Using Modern Design Rules.*

Filipp Akopyan (M.S. EE, August 2005). *Asynchronous Analog-to-Digital Conversion.*

David Fang (M.S. EE, October 2003). *Designing Asynchronous Register Files.*

David Biermann (M.S. EE, December 2002). *Multiprocessor-Enabled Asynchronous Cache Controller.*

Clinton Kelly IV (M.S. EE, November 2002). *Wireless Network Simulation Done Faster than Real Time.*

Virantha Ekanayake (M.S. EE, November 2002). *Asynchronous DRAM Design and Implementation.*

John Teifel (M.S. EE, May 2002). *Interchip Communication in Asynchronous VLSI Systems.*

Senior projects supervised:

Bryan Herbert (B.S. EE, May 2018). *Beating the Ethereum Blockchain: An Optimized Memory Architecture for the Ethash PoW Algorithm.*

Pravat Trairatvorakul (B.S. EE/CS, May 2018). *CHARM: CHip Automated Routing Module for Magic VLSI.*

Eli Baum (B.S. EE/CS, May 2019). *Dynamic translation.*

Christina Huang (B.S. EE/CS, May 2019). *Wireless sensor monitoring.*

Rishab Ramanathan (B.S. EE/CS, May 2019). *Transistor sizing for asynchronous circuits.*

Lilium Wu (B.S. CS, May 2019). *Wireless sensor monitoring.*

Patrick Lawe (B.S. EE/CS, May 2019). *Comparing Stochastic Computing Logic.*

David Schwartz (B.S. CS/Econ, May 2019). *A utility function for Circuit design.*

Zeb Mehring (B.S. EE/CS, May 2019). *Syntax-directed translation of CHP programs.*

Sabrina Long (B.S. CS, Dec 2019). *Real-time 3D object tracking.*

Carlo Abelli (B.S. CS, May 2020). *A RISC-V emulator.*

Abhinand Sivaprasad (B.S. CS, May 2020). *A RISC-V emulator.*

Edmund Chute (B.S. CS, May 2020). *Voice-based control of embedded systems using Alexa.*

Amanda Hansen (B.S. EE/CS, May 2020). *Optimizing syntax-directed translation of CHP programs.*

⋆ Cornell nominee for the ACM Doctoral Dissertation Award in Computer Science.

Nicholas Herrera (B.S. CS, May 2020). *A Zero-Touch Digital System for Creating Analog Visual Works.*

Lincoln Berkley (B.S. EE/CS, May 2021). *Dataflow optimization of asynchronous circuits.*

Kevin Choi (B.S. EE/CS, May 2021). *An asynchronous SPI interface.*

Bowen Du (B.S. CS, May 2021). *Database-backed web applications.*

Adam Wolnikowski (B.S. EE/CS, May 2021). *Zero-copy serialization.*

Mawuli Akpalu (B.S. EE/CS, May 2022). *Eclipse-based ACT editor.*

Blaise Fangman (B.S. EE/CS, May 2022). *Asynchronous memory in OpenRAM.*

Zach Taylor (B.S. EE/CS, May 2023). *RISCV-Matrix: a vectorized library for advanced matrix manipulation.*

Henry Heffan (B.S. CS, May 2023). *OCaml ACT.*

Ansel Bobrow (B.S. CS, May 2024). *Level Crossing Sampling.*

Ben Goldstein (B.S. CS, May 2024). *Parasitic extraction for VLSI Circuits.*

Vaibhav Sharma (B.S. CS, May 2024). *Smart Glasses.*

Connor Mann (B.S. CS, May 2024). *Bluetooth Low Energy Web API.*

Rylan Polster (B.S. EE/CS, May 2025). *Converting Handshaking Expansions to Production Rules for Asynchronous VLSI.*

Alex Shin (B.S. EE/CS, May 2025). *Vision-Enhanced Smart Glasses for Real-Time American Sign Language to Speech Translation using Deep Learning.*

Alex Johnson (B.S. EE/CS, May 2025). *Event-driven imagers.*

Siva Nalabothu (B.S. Neuroscience and CS/Econ, May 2025). *Asynchronous Neuromorphic Processor for Artificial Neural Networks in a Brain-Computer Interface as a Model for a Theory of Human Intelligence.*

External committees/advising/reviewer for graduate students:

Mika Nyström. *Asynchronous Pulse Logic*. Ph.D. CS, California Institute of Technology (2001). Advisor: Alain J. Martin

Saber Moradi. *Memory-efficient Circuits and Architectures for Asynchronous Neuromorphic Systems*. Ph.D. EE, ETH Zurich (2014). Advisor: Giacomo Indiveri

Peter Diehl. *Performant Spiking Systems*. Ph.D. EE, ETH Zurich (2016). Advisor: Matthew Cook

Yu Chen. *Digital Signal Processing with Signal-Derived Timing: Analysis and Implementation.* Ph.D. EE, Columbia University (2016). Advisor: Yannis Tsividis

Alexander Neckar. *Brainstorm: A Mixed-Signal Brain-inspired Architecture with a Dynamical Systems-based Programming Model.* Ph.D. EE, Stanford (2018). Advisor: Kwabena Boahen

Sam Folk. *Computation and Communication with Spikes in Neuromorphic Systems.* Ph.D. EE, Stanford (2018). Advisor: Kwabena Boahen

Nitish Srivastava. *Design and Generation of Efficient Hardware Accelerators for Tensor Computation.* Ph.D. ECE, Cornell University (2020). Advisors: David Albonesi, Zhiru Zhang

Yi-Shan Lu. *Effectively Parallelizing Electronic Design Automation Algorithms Using the Operator Formulation.* Ph.D. CS, University of Texas at Austin (2022). Advisor: Keshav Pingali

Michael He. *Detailed-routability-driven and Timing-driven Scalable Parallel Global Routing.* Ph.D. CS, University of Texas at Austin (2022). Advisor: Keshav Pingali

Naomi Sagan. *Ising Machines: Theory and Practice* M.S. EECS, University of California at Berkeley (2023). Advisor: Jaijeet Roychowdhury

Zhe Su. *Design Principles for Energy and Memory Efficient Neuromorphic Architectures.* Ph.D. EE, ETH Zurich (2025). Advisor: Giacomo Indiveri

Leo Liu. *TBD.* Ph.D. EE, Stanford University. Advisor: Kwabena Boahen

University Service:

Yale:

Department:

Faculty recruiting:

ECE Microelectronics Faculty search committee, 2024–2026
EE Microelectronics and Computer Engineering Faculty search committee, 2022–2024
Chair, EE Computer Engineering Faculty search committee, 2018–2019, 2021–2022, 2023–2024
EE Senior Faculty search committee, 2018–2019
CS Systems Faculty search committee, 2019–2020

Other:

Director of Undergraduate Studies (EECS major), 2021–
EE Graduate admissions (computer engineering area), 2018–

University:

Chair, Yale Center for Research Computing Faculty Advisory Committee, 2024–
Deputy Dean, School of Engineering and Applied Science (SEAS)
Innovation and Entrepreneurship, 2024–
Research, 2023–2024
Physical Sciences & Engineering Area/Tenure Appointments Committee, 2018–20, 2023–
Wu-Tsai Institute Steering Committee, 2023–24, 2025–26
Yale Ventures Advisory Board, 2022–26
Faculty Standards Review Committee, 2022–23
Academic Resource Committee, SEAS 2022–
Wu-Tsai Institute Faculty search committee, 2021–24, 2025–26
Wu-Tsai Institute Working Group on Neurocomputing and Machine Intelligence, 2021
Yale Instrumentation Steering Committee, 2019–20
Yale Center for Research Computing Steering Committee, 2019–20
Export Control Advisory Board, 2019–20
Faculty of Arts and Sciences Senate, 2017–19 (executive committee, 2017–19)
Cooperative Research Committee, 2017–22

Science and Engineering Planning:

Robotics Working Group, SEAS 2022–2023
Strategic Vision Implementation Committee, SEAS 2022–
Data Science Advisory Group, 2021–22
Physical Science and Engineering Building Planning Committee, 2020–
Strategic Planning Committee for SEAS, 2020–2021
Physical Science and Engineering Building Instrumentation Task Force, 2020–2021
Science of Data Working Group, 2019–20
Panel member for Computer Science, University Science Strategy Committee, 2017–2018

Cornell:

Department:

Faculty recruiting:

ECE Faculty Search Committee for NYC faculty, 2012–2014
Faculty recruiting oversight committee, Jacobs Technion-Cornell Innovation Institute, 2013–2014
CS Faculty Search Committee, 2008–2012
Search Committee for ECE Director, 2007–2008, 2013–2014

ECE Targeted Faculty Recruiting Committees, 1998–2001, 2003–2006, 2008
ECE General Faculty Recruiting Committee, 2001–2003, 2008–2010

Graduate programs:
Academic Program Director, Computer Science M.Eng. program, Cornell Tech, 2013–14
Director of Graduate Studies, ECE, 2007–2009
ECE Graduate Committee, 1999–2001, 2003–2004

Other:
Ad hoc committee member and chair for faculty promotions and reappointments (multiple)
ECE Policy Committee, 2001–2004, vice chair 2004–2005
CAM Computer Committee, Chair 2001–2004
ECE Computing Committee, 1999–2001

University:

Major roles:
Associate Dean for Research, Cornell Tech, 2015
Associate Dean for Academic Affairs, Cornell Tech, 2012–2014
Co-Chair, Academic Planning Committee for Cornell Tech, 2012–2013
Associate Dean for Research and Graduate Studies in Engineering, 2010–2012

Technology transfer and conflict of interest:
Financial Conflict of Interest Committee, 2013–2016
Technology Transfer Advisory Committee, 2008–2013
Operations oversight subcommittee for technology transfer office, 2008–2013
Mediation subcommittee for grievances, 2008–2013

Recruiting senior staff:
Search committee for the Director of Cornell's Center for Technology Licensing, 2015
Search committee for the Director of Cornell's Sponsored Programs Office, 2010, 2013

Graduate studies:
Graduate Education Planning Task Force, 2009
Research Advisory Group for Engineering, 2008–2009
Review committee, Graduate School TOEFL Requirements, 2008–2012
Graduate Admissions Advisory Board, 2005

Teaching:
Advisory Board Member, Center for Teaching Excellence, 2011–2013
College of Engineering Teaching Awards Committee, 2003

PUBLICATIONS

(underlined names are members of my research group)

Book Chapter Contributions:

Neuro-Symbolic Computing: Hardware-Software Co-Design. Chapter 11 in "Neuro-symbolic AI: Foundations and Applications," 2026. (A summary of a collection of talks)

Asynchronous FPGAs. Chapter 12 in "Asynchronous Circuit Applications," Institute of Engineering and Technology, 2019.

Communication. Chapter 2 in "Event-based Neuromorphic Systems." Wiley, 2015.

Towards Large-Scale Neuromorphic Systems. Chapter 16 in "Event-based Neuromorphic Systems." Wiley, 2015.

Articles:

Rajit Manohar. Self-timed systems for energy-efficient computing. To appear, *Philosophical Transactions of the Royal Society A*.

Amirmohammad Nazari, Rajit Manohar, Robert Soulé. Accio: Rethinking OS-Architecture Co-Design for Next-Gen I/O. *New Ideas in Networked Systems*, February 2026.

Congyang Li, Nabil Imam, and Rajit Manohar. A deterministic neuromorphic architecture with scalable time synchronization. *Nature Communications*, **16**(1):10329, 2025.

Venkata Pavan Sumanth Sikhakollu, Shreesha Sreedhara, Thomas Jagielski, Gagan Deep Goru, Jui-Hsin Hung, Rajit Manohar, and Jaijeet Roychowdhury. DOIM50: A 50-Spin Fully Connected Oscillator Ising Machine IC for MU-MIMO Detection. *International Symposium on Nonlinear Theory and Its Applications*, October 2025. (**Best paper nominee**)

Abhishek Bhattacharjee, Quanquan C. Liu, Rajit Manohar, Raghavendra Pothukuchi, and Muhammed Ugur. Dataflow-Specific Algorithms for Resource-Constrained Scheduling and Memory Design. *ACM Symposium on Parallelism in Algorithms and Architectures*, July 2025.

Karthi Srinivasan and Rajit Manohar. Maelstrom: A Logic Synthesis Technique for Asynchronous Circuits. Accepted, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*.

Rui Li, Lincoln Berkley, and Rajit Manohar. PipeLink: A Pipelined Resource Sharing System for Dataflow High-level Synthesis. *IEEE/ACM Design Automation Conference*, June 2025.

Xiayuan Wen, Rui Li, and Rajit Manohar. Translating General Slack Elastic Programs into Dataflow Circuits *Proceedings of the IEEE International Symposium on Asynchronous Circuits and Systems*, May 2025.

Karthi Srinivasan and Rajit Manohar. Automated Decomposition of Concurrent Programs for Asynchronous Logic Synthesis. *Proceedings of the IEEE International Symposium on Asynchronous Circuits and Systems*, May 2025.

Prafull Purohit and Rajit Manohar. Asynchronous, event-driven readout for large-scale imaging devices. *Proceedings of the IEEE International Symposium on Asynchronous Circuits and Systems*, May 2025.

Ruslan Dashkin and Rajit Manohar. Mixed-Level Emulation of Asynchronous Circuits on Synchronous FPGAs. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **44**(4):1516–1528, April 2025.

Jason Yik et al. (community "perspectives" article; full author list at end of document) The neurobench framework for benchmarking neuromorphic computing algorithms and systems. *Nature Communications*, **16** 1545, February 2025.

Raghavendra Pothukuchi, Karthik Sriram, Michal Gerasimiuk, Muhammed Ugur, Rajit Manohar, Anurag Khandelwal, Abhishek Bhattacharjee. Distributed Brain-Computer Interfacing with a Networked Multi-Accelerator Architecture. *IEEE Micro Special Issue: Micro's Top Picks from Architecture Conferences*, 2024. (Original paper: "SCALO: An Accelerator-Rich Distributed System for Scalable Brain-Computer Interfacing").

Venkata Pavan Sumanth Sikhakollu, Shreesha Sreedhara, Rajit Manohar, Alan Mishchenko, and Jaijeet Roychowdhury. High Quality Circuit-based 3-SAT Mappings for Oscillator Ising Machines. *International Conference on Unconventional Computation and Natural Computation*, June 2024.

Mattia Vezzoli, Lukas Nel, Kshitij Bhardwaj, Rajit Manohar and Maya Gokhale. Designing an Energy-Efficient Fully-Asynchronous Deep Learning Convolution Engine. Late-breaking results, *Design Automation and Test in Europe (DATE)*, March 2024.

Xiaoxuan Yang, Zhangyang Wang, X Sharon Hu, Chris H Kim, Shimeng Yu, Miroslav Pajic, Rajit Manohar, Yiran Chen, Hai Helen Li. Neuro-Symbolic Computing: Advancements and Challenges in Hardware-Software Co-Design. *IEEE Transactions on Circuits and Systems II*, **71**(3):1683–1689, March 2024.

Noa Zilberman, Eve M. Schooler, Uri Cummings, Rajit Manohar, Dawn Nafus, Robert Soulé, Rick Taylor. Toward Carbon-Aware Networking. *ACM SIGENERGY Energy Informatics Review (EIR)*, October 2023.

Rajit Manohar and Yoram Moses. Timed Signalling Processes. *Proceedings of the IEEE International Symposium on Asynchronous Circuits and Systems*, July 2023. (**Best paper award**)

Xiang Wu and and Rajit Manohar. Verification-driven Design for Asynchronous VLSI. *Proceedings of the IEEE International Symposium on Asynchronous Circuits and Systems*, July 2023.

Karthi Srinivasan, Yoram Moses, and Rajit Manohar. Opportunistic Mutual Exclusion. *Proceedings of the IEEE International Symposium on Asynchronous Circuits and Systems*, July 2023. (**Best paper nominee**)

Prafull Purohit, Johannes Leugering, and Rajit Manohar. An Efficient Data Structure for Sparse Bit-Vectors with Applications in Neuromorphic Computing. *Proceedings of the IEEE International Symposium on Asynchronous Circuits and Systems*, July 2023.

Abhishek Bhattacharjee, Rajit Manohar, Karthik Sriram. RETROSPECTIVE: Hardware-Software Co-Design for Brain-Computer Interfaces. *ISCA@50 Retrospective*, June 2023. (**ISCA-50 25-year retrospective**)

Karthik Sriram, Raghavendra Pothukuchi, Michal Gerasimiuk, Muhammed Ugur, Oliver Ye, Rajit Manohar, Anurag Khandelwal, Abhishek Bhattacharjee. SCALO: An Accelerator-Rich Distributed System for Scalable Brain-Computer Interfacing. *IEEE/ACM International Symposium on Computer Architecture*, June 2023. (**Best paper award**, **IEEE Micro Top Picks 2024**)

Ioannis Karageorgos, Karthik Sriran, Xiayuan Wen, Jan Vesely, Nick Lindsay, Michael Wu, Lenny Kazan, Raghavendra Pothukuchi, Rajit Manohar, and Abhishek Bhattacharjee. HALO: A Hardware-Software Co-Designed Processor for Brain-Computer Interfaces. *IEEE Micro*, Special issue from the HotChips 2022 conference, **43**:64–72, May-June 2023.

Dan Li, Marie Brault, Rajit Manohar, Sten Vermund, Ashley Hagaman, Laura Forastiere, Tyler Caruthers, Emilie Egger, Yizhou Wang, Nathan Manohar, Peter Manohar, J Lucian Davis, and Xin Zhou. Implementation of a Hardware-Assisted Bluetooth-Based COVID-19 Tracking Device in a High School: Mixed Methods Study. *JMIR Formative Research*, **7**(1), April 2023.

Prafull Purohit and Rajit Manohar. Field-programmable encoding for address-event representation. *Frontiers in Neuroscience*, **16**, December 2022.

Ruslan Dashkin and Rajit Manohar. General Approach to Asynchronous Circuits Simulation Using Synchronous FPGAs. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **41**(10):3452–3465, October 2022.

Ioannis Karageorgos, Karthik Sriran, Jan Vesely, Michael Wu, Xiayuan Wen, Nick Lindsay, Lenny Kazan, Rajit Manohar, and Abhishek Bhattacharjee. HALO: A Flexible and Low Power Processing Fabric for Brain-Computer Interfaces. *HotChips 2022: Workshop on High-Performance Chips*, August 2022.

Rajit Manohar. Hardware/software co-design for Neuromorphic Systems. *Proceedings of the IEEE Custom Integrated Circuits Conference*, April 2022. (Invited)

Jiayuan He, Udit Agarwal, Yihang Yang, Rajit Manohar, Keshav Pingali. SPRoute 2.0: A detailed-routability-driven deterministic parallel global router with soft capacity. *Proc. 27th Asia and South Pacific Design Automation Conference*, Jaunary 2022.

Tyler Shelby, Tyler Caruthers, Oren Kanner, Rebecca Schneider, Dana Lipnickas, Lauretta Grau, Rajit Manohar, Linda Niccolai. Pilot Evaluations of Two Bluetooth Contact Tracing Approaches on a University Campus: Mixed Methods Study. *JMIR Formative Research*, **5**(10), October 2021.

Prafull Purohit and Rajit Manohar. Hierarchical Token Rings for Address-Event Encoding. *Proceedings of the IEEE International Symposium on Asynchronous Circuits and Systems*, September 2021.

Rui Li, Lincoln Berkley, Yihang Yang, and Rajit Manohar. Fluid: An Asynchronous High-level Synthesis Tool for Complex Program Structures. *Proceedings of the IEEE International Symposium on Asynchronous Circuits and Systems*, September 2021. (**Best paper nominee**)

Adam Wolnikowski, Stephen Ibanez, Jonathan Stone, Changhoon Kim, Rajit Manohar, Robert Soule. Zerializer: Towards Zero-Copy Serialization. *18th Workshop on Hot Topics in Operating Systems*, May/June 2021.

Karthik Sriram, Ioannis Karageorgos, Jan Vesely, Nick Lindsay, Xiayuan Wen, Michael Wu, Marc Powell, David Borton, Rajit Manohar, Abhishek Bhattacharjee. Balancing Specialized Versus Flexible Computation in Brain-Computer Interfaces. *IEEE Micro Special Issue: Micro's Top Picks from Architecture Conferences*, 2021. (Original paper: "Hardware-Software Co-Design for Brain-Computer Interfaces").

Samira Ataei, Wenmian Hua, Yihang Yang, Rajit Manohar, Jiayuan He, Yi-Shan Lu, Sepideh Maleki, Keshav Pingali. An Open-Source EDA flow for Asynchronous Logic. *IEEE Design & Test Special Issue: Open-source EDA*, 2021.

Ned Bingham and Rajit Manohar. A Systematic Approach for Arbitration Expressions. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **67**(12):4960–4969, December 2020.

Yihang Yang, Michael He, and Rajit Manohar. Dali: A gridded cell placement flow. *International Conference on Computer-Aided Design*, November 2020.

Rajt Manohar. Exact Timing Analysis for Asynchronous Circuits with Multiple Periods. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **39**(10):3134–3138, October 2020.

Ioannis Karageorgos, Karthik Sriram, Jan Vesely, Michael Wu, Marc Powell, David Borton, Rajit Manohar, and Abhishek Bhattacharjee. Hardware-Software Co-Design for Brain-Computer Interfaces. *IEEE/ACM International Symposium on Computer Architecture*, June 2020. (**IEEE Micro Top Picks 2021**)

Wenmian Hua, Yi-Shan Lu, Keshav Pingali, and Rajit Manohar. Cyclone: A static timing and power engine for asynchronous circuits. *IEEE International Symposium on Asynchronous Circuits and Systems*, May 2020. (**Best paper award**)

Samira Ataei and Rajit Manohar. Shared-staticizer for area-efficient asynchronous circuits. *IEEE International Symposium on Asynchronous Circuits and Systems*, May 2020.

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